D1 integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

REMARKS

The above changes to the language of claim 73 clarify that claim and eliminate an inadvertent lack of antecedent basis problem in the former wording of the claim.

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500. Shortly before issuing the Office Action, the Examiner had called to indicate that certain claims were allowable over the prior art, but when the undersigned attorney returned the Examiner's call, it was indicated that new prior art had been found and that a new action would be forthcoming. It is assumed that the Magar reference relied on is that new prior art. A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.

X

The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention. The crystal clock 434 is thus used in the invention for synchronizing I/O timing with the outside world, while the ring counter variable speed clock 430 also shown in Figure 17 is used for generating on-chip clock signals. The clock 430 is an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate.

The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the "conventional crystal clock" 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar:

> "The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of Fig. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate for quarter-cycle clocks Q1, Q2, Q3 and Q4, seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state of time of 200 ns., minimum; the states are referred to as S0, S1, S2 in FIG 3. The clock generator produces an output CLKOUT, Fig. 3f, on one of the control bus lines 13. CLKOUT has the same period as

> Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external components of the system of FIG. 1."

This description in Magar should be contrasted with the following detailed description of an embodiment of the present invention, as shown in Fig. 17, at explained at page 32, lines 3-29:

> "Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in Figure 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (Figure 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436, with data/addresses passing on bus 90, 136."

From these two quotations, it is clear that the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430, and that Magar is merely representative of the "most microprocessors" acknowledged as prior art in the above description from the present application, which prior art microprocessors use a "conventional crystal clock." Because the variable speed clock is a primary point of departure from the prior art, independent claims 19, 65, 73 and 78 all recite a system including a variable speed clock or a method including using a variable speed clock. In light of the prior art, of which Magar is a good example, Applicants are entitled to claims of this scope. Dependent claims 20, 66, 74 and 79 further recite a second clock, exemplified by the crystal clock 434 in Fig. 17.

Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is

frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. Conventionally, a CPU is driven by a clock that is generated by an crystal. The crystal might be connected directly to two pins on the CPU, as in Magar, and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. Alternatively, the crystal may be contained in a package with the oscillation circuitry, the packaged component thus called an oscillator, and connected to one pin on the CPU as in Edwards et al., U.S. Patent 4,680,698.

While an oscillator may be a clock, a clock is not usually an oscillator. An oscillator must exist someplace in the circuit from which a periodic clock is derived. In both cases, the crystal (or the entire oscillator in the second case) is external to the CPU, and the output of the oscillator circuitry is a "clock." This clock is typically modified to produce additional required clock signals for the system. The many clock signals are sometimes created by circuitry called a "clock generator." For example, see Magar, Fig. 2a. The "clock gen" connects to a crystal at external pins X1 and X2 and generates clock signals for the system Q1, Q2, Q3, Q4 and CLKOUT. Other cited reference have similar examples, see Palmer, U.S. Patent 4,338,675, Fig. 1, item 24; Pohlman et al., U.S. Patent 4, 112,490 Fig. 1, item 22. All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture. Because of the cutting and trimming required, and that the crystal slice is typically suspended by two wires to allow it to freely oscillate, crystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

Note that the term clock can refer to many different signals since the definition is broad, and that it can also refer to the oscillator that is required to generate the clock. While a crystal-controlled oscillator typically operates at a single speed, the circuitry around the crystal may be

designed so that the output of the entire oscillator circuit can be varied. Many mechanisms can be used to control the output of a variable-frequency oscillator, including manual inputs, program-controlled inputs, temperature sensors, or other devices. Non-crystal controlled oscillators are also possible, and when they are designed as variable-frequency oscillators they are typically also controlled by manual inputs, program-controlled inputs, temperature sensors and other devices.

The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so. Like the cited references, the driven device might additionally contain clock generation circuitry to produce variations on the clock output of the oscillator or variable speed clock for the other circuitry on the device.

The remaining Bennett et al., Brantingham, Pollack, Gruner et al.and Suzuki et al. references, cited but not applied in a rejection, have been reviewed and found not pertinent to the invention as claimed.

Based on the above remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

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